# RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

**Data Sheet** **February 2005**

## 70A, 60V, 0.014 Ohm, N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA78440.

## Ordering Information

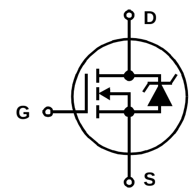
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RFG70N06 | TO-247 | RFG70N06 |
| RFP70N06 | TO-220AB | RFP70N06 |
| RF1S70N06 | TO-262AA | F1S70N06 |
| RF1S70N06SM | TO-263AB | F1S70N06 |

NOTE: When ordering use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N06SM9A.

## Features

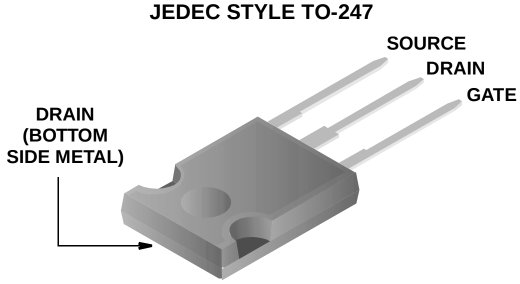
- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- Temperature Compensated PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- 175$^o$C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

## Symbol

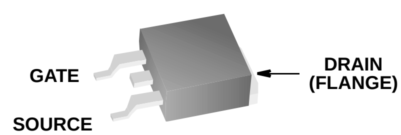



## Packaging

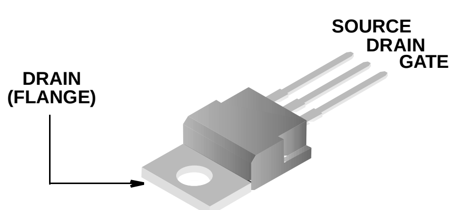
JEDEC STYLE TO-247



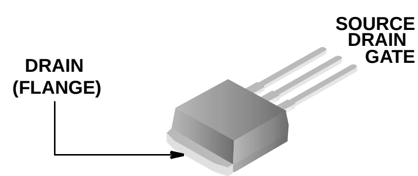

JEDEC TO-263AB




JEDEC TO-220AB




JEDEC TO-262AA



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | RFG70N06, RFP70N06 RF1S70N06, RF1S70N06SM | UNITS |
|---|---|---|
| Drain to Source Voltage (Note 1) . . . . . $V_{DSS}$ | 60 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) . . . . . $V_{DGR}$ | 60 | V |
| Continuous Drain Current . . . . . $I_D$ | 70 | A |
| Pulsed Drain Current (Note 3) . . . . . $I_{DM}$ | Refer to Peak Current Curve | |
| Gate to Source Voltage . . . . . $V_{GS}$ | ±20 | V |
| Single Pulse Avalanche Rating . . . . . $E_{AS}$ | Refer to UIS Curve | A |
| Power Dissipation . . . . . $P_D$ | 150 | W |
| Linear Derating Factor . . . . . | 1.0 | W/$^o$C |
| Operating and Storage Temperature . . . . . $T_J$, $T_{STG}$ | -55 to 175 | $^o$C |
| Maximum Temperature for Soldering | | |
| Leads at 0.063in (1.6mm) from Case for 10s. . . . . $T_L$ | 300 | $^o$C |
| Package Body for 10s, See Techbrief 334 . . . . . $T_{pkg}$ | 260 | $^o$C |

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $150^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250µA, $V_{GS}$ = 0V (Figure 11) | | 60 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = 250µA (Figure 10) | | 2 | - | 4 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60V, $V_{GS}$ = 0V | | - | - | 1 | µA |
| | | $V_{DS}$ = 0.8 x Rated $BV_{DSS}$, $T_C = 150^oC$ | | - | - | 25 | µA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | | - | - | ±100 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $I_D$ = 70A, $V_{GS}$ = 10V (Figure 9) | | - | - | 0.014 | Ω |
| Turn-On Time | $t_{(ON)}$ | $V_{DD}$ = 30V, $I_D \approx$ 70A, $R_L$ = 0.43Ω, $V_{GS}$ = 10V, $R_{GS}$ = 2.5Ω (Figure 13) | | - | - | 190 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 10 | - | ns |
| Rise Time | $t_r$ | | | - | 137 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 32 | - | ns |
| Fall Time | $t_f$ | | | - | 24 | - | ns |
| Turn-Off Time | $t_{(OFF)}$ | | | - | - | 73 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 20V | $V_{DD}$ = 48V, $I_D$ = 70A, $R_L$ = 0.68Ω $I_{g(REF)}$ = 2.2mA (Figure 13) | - | 120 | 156 | nC |
| Gate Charge at 10V | $Q_{g(10)}$ | $V_{GS}$ = 0V to 10V | | - | 65 | 85 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 2V | | - | 5.0 | 6.5 | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz (Figure 12) | | - | 2250 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 792 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 206 | - | pF |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | | | - | - | 1.0 | $^o$C/W |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | TO-220 and TO-263 | | - | - | 62 | $^o$C/W |
| | | TO-247 | | - | - | 30 | $^o$C/W |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 70A | | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 70A, $dI_{SD}/dt$ = 100A/µs | | - | 52 | ns |

NOTES:

2. Pulse test: pulse width ≤300ms, duty cycle ≤2%.
3. Repetitive rating: pulse width is limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3) and Peak Current Capability Curve (Figure 5).

## Typical Performance Curves
$T_C = 25^oC$, Unless Otherwise Specified

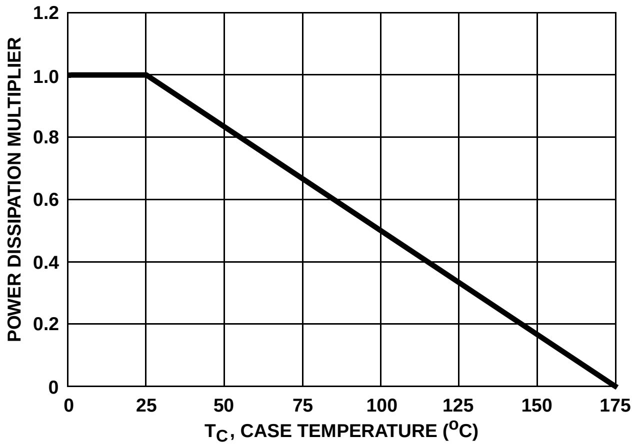



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

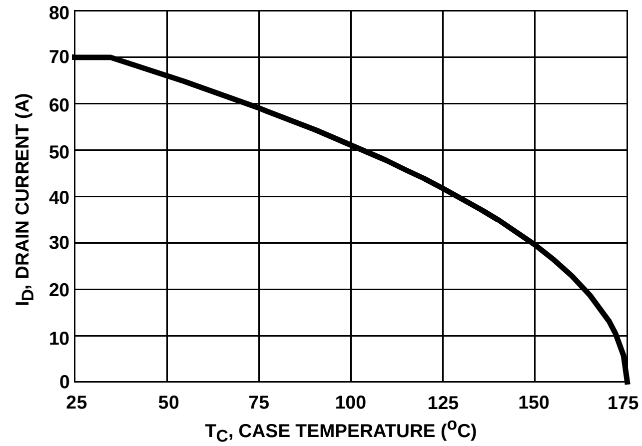



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

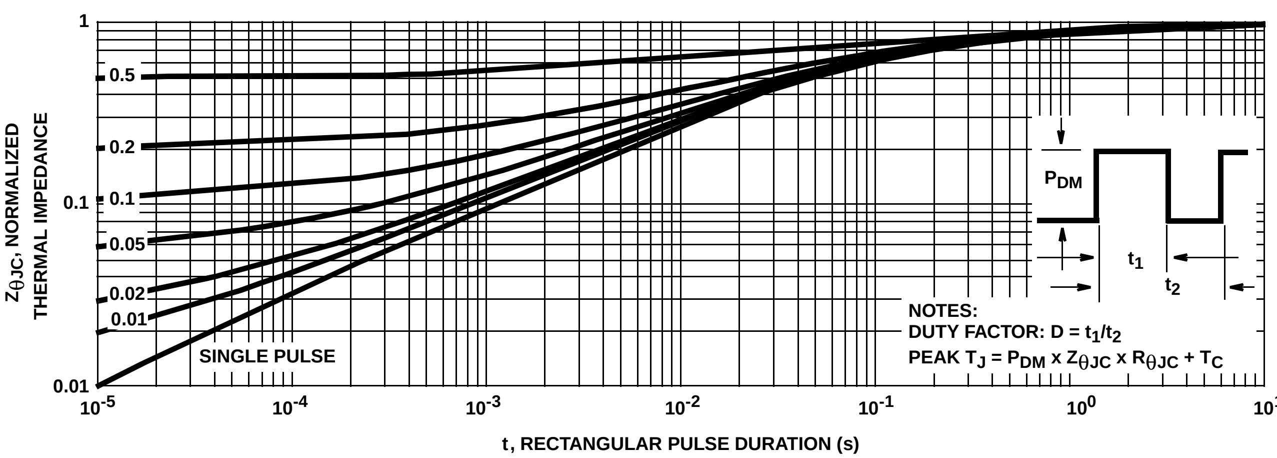



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

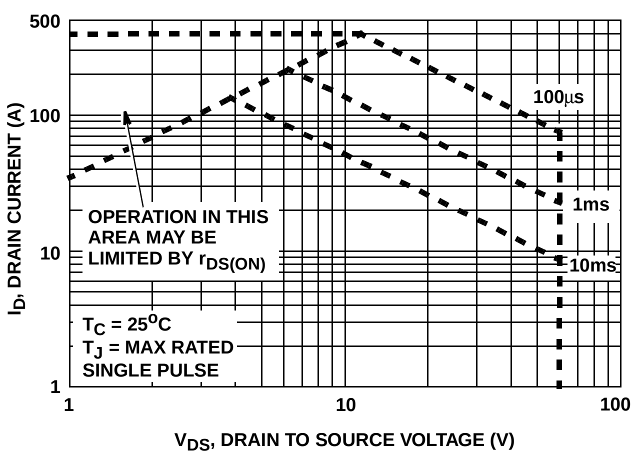



FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

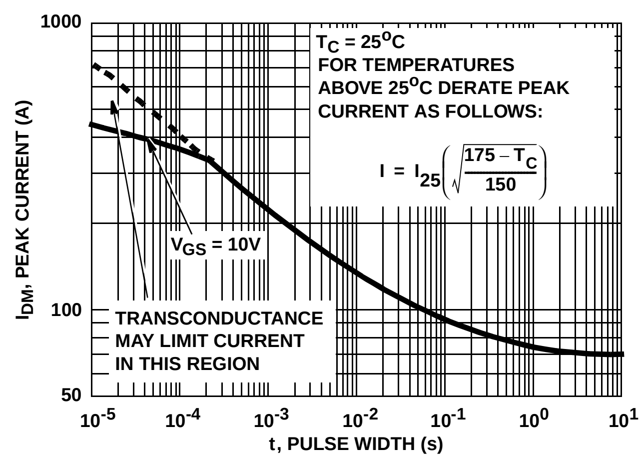
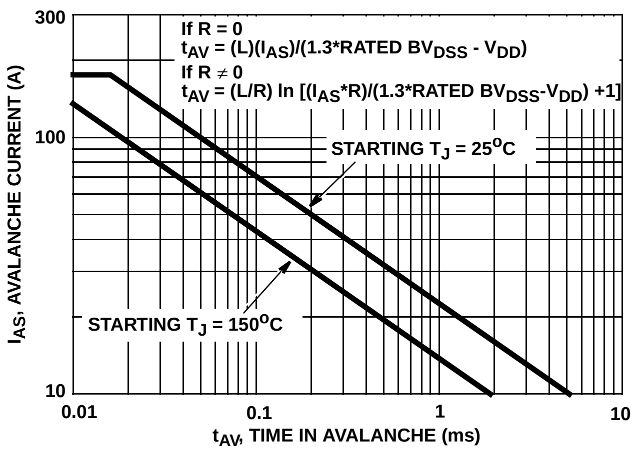



FIGURE 5. PEAK CURRENT CAPABILITY

## *Typical Performance Curves* $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**




NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

**FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**

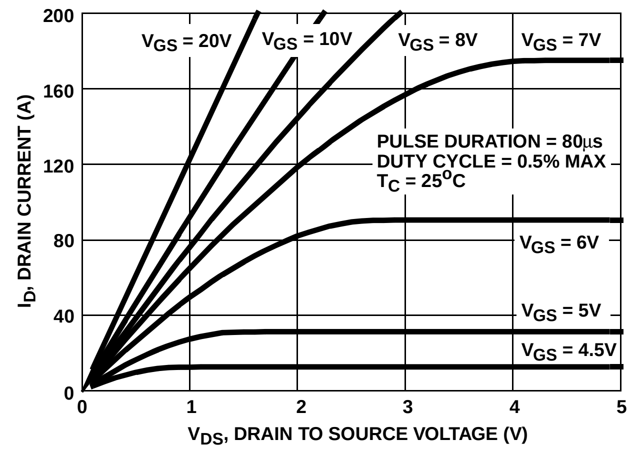



**FIGURE 7. SATURATION CHARACTERISTICS**

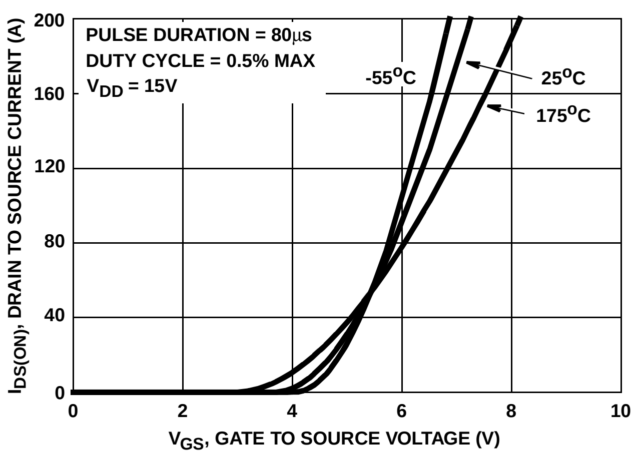



**FIGURE 8. TRANSFER CHARACTERISTICS**

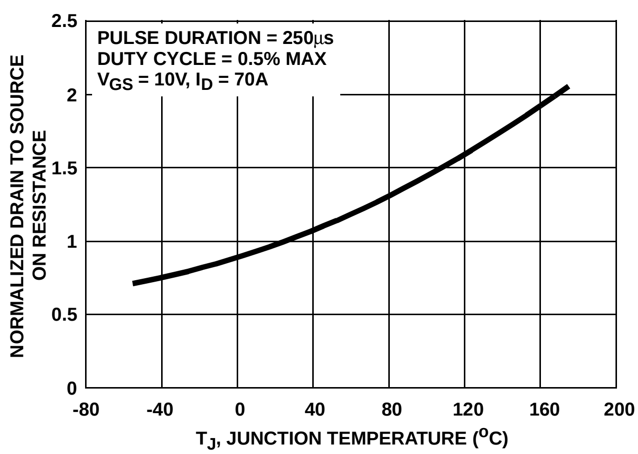



**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**

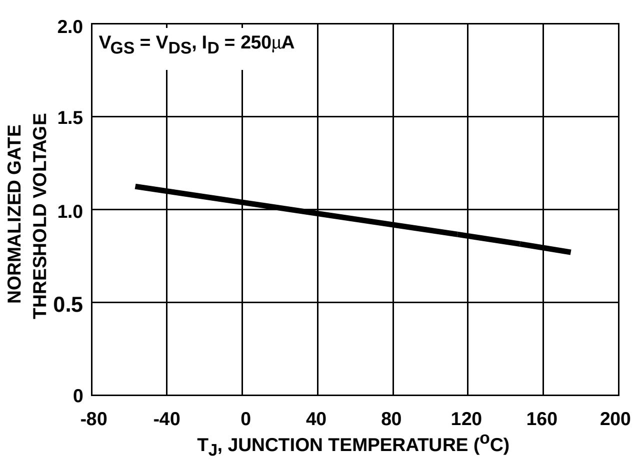



**FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE**

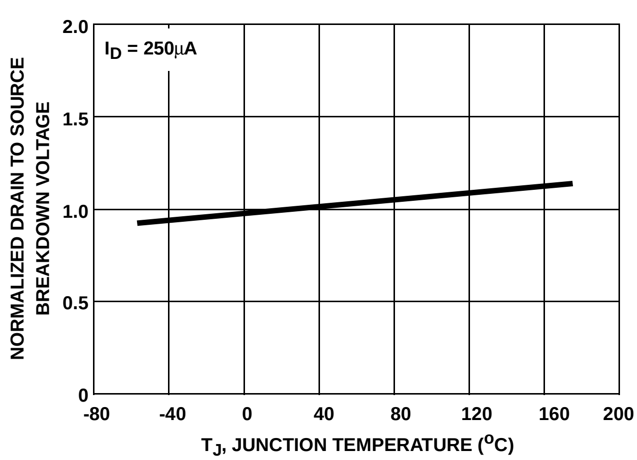



**FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE**

## Typical Performance Curves $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

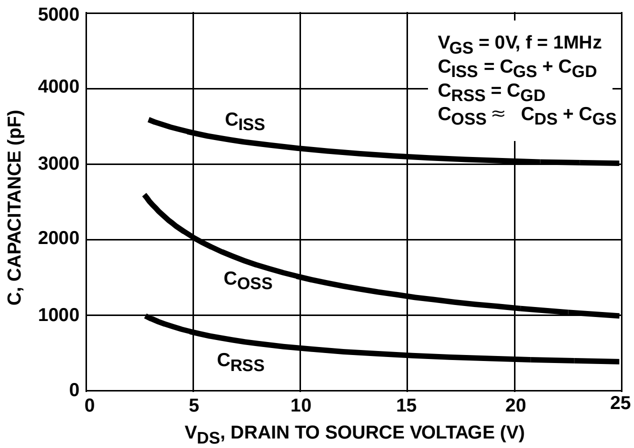
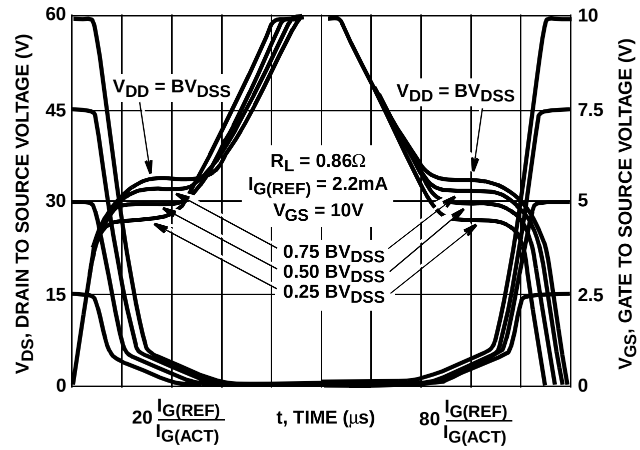



FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

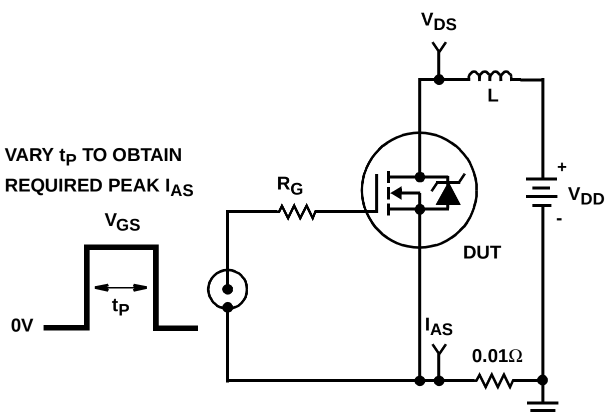



FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

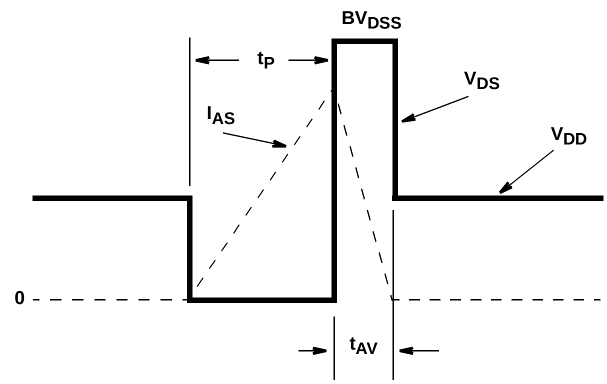



FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

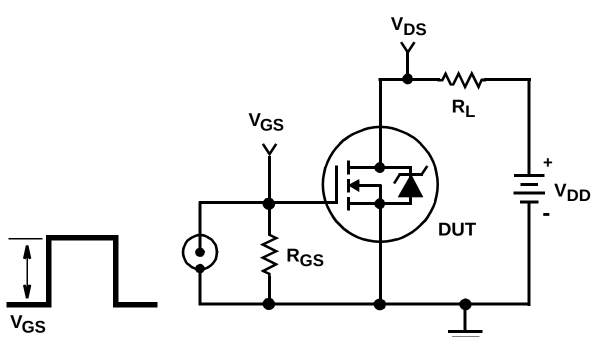



FIGURE 16. SWITCHING TIME TEST CIRCUIT

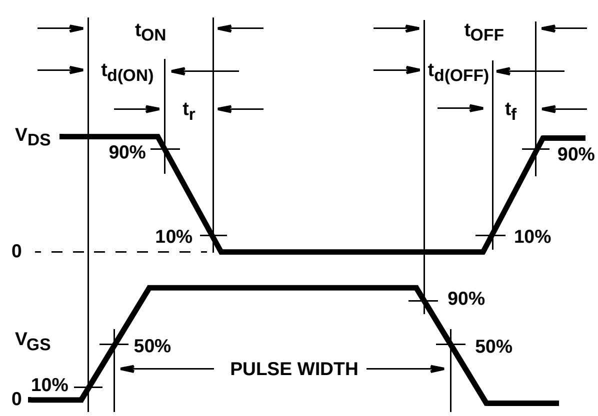



FIGURE 17. SWITCHING WAVEFORMS

## Test Circuits and Waveforms (Continued)

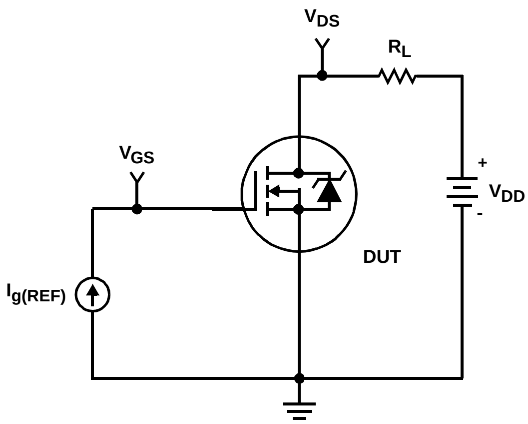



FIGURE 18. GATE CHARGE TEST CIRCUIT

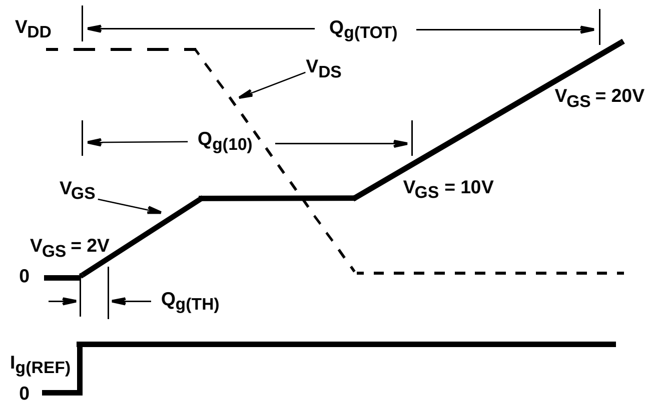



FIGURE 19. GATE CHARGE WAVEFORM

## *PSPICE Electrical Model*

```
.SUBCKT  RFG70N06  2 1 3 ;       rev 3/20/92

CA  12  8  5.56e-9
CB  15  14  5.30e-9
CIN  6  8 2.63e-9

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  65.18
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

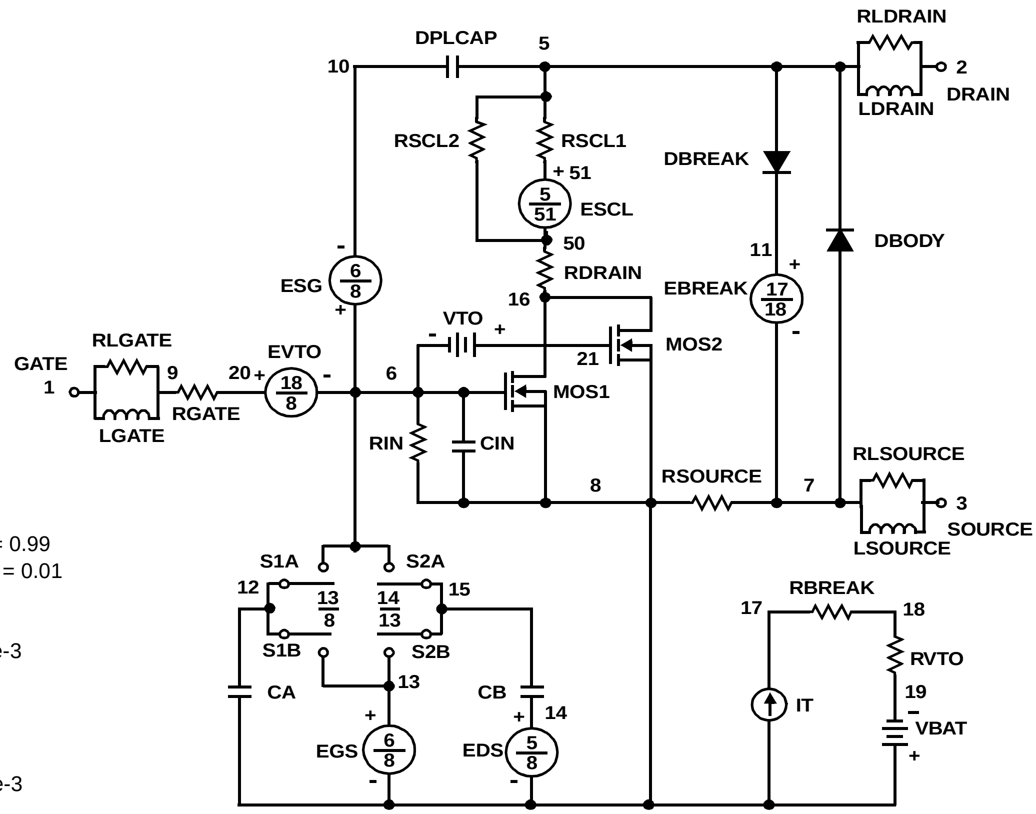
LDRAIN  2  5  1e-9
LGATE 1  9  3.10e-9
LSOURCE  3  7  1.82e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  50  16  RDSMOD  4.66e-3
RLDRAIN  2  5  10
RGATE  9  20  1.21
RLGATE 1  9  31
RIN  6  8  1e9
RSOURCE  8  7  RDSMOD  3.92e-3
RLSOURCE  3  7  18.2
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6   0.605
```




```
.MODEL DBDMOD D (IS = 7.91e-12  RS = 3.87e-3  TRS1 = 2.71e-3  TRS2 = 2.50e-7  CJO = 4.84e-9  TT = 4.51e-8)
.MODEL DBKMOD D (RS = 3.9e-2  TRS1 =1.05e-4  TRS2 = 3.11e-5)
.MODEL DPLCAPMOD D (CJO = 4.8e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 3.46  KP = 47  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 8.46e-4  TC2 = -8.48e-7)
.MODEL RDSMOD RES (TC1 = 2.23e-3  TC2 = 6.56e-6)
.MODEL RVTOMOD RES (TC1 = -3.29e-3  TC2 = 3.49e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -8.35  VOFF= -6.35)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.35  VOFF= -8.35)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.0  VOFF= 3.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 3.0  VOFF= -2.0)

.ENDS
```

NOTE:  For further discussion of  the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

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